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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,266	05/20/2004	Dominik J. Schmidt	IVT.0033US	4584

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EXAMINER	
PHAN, DEAN	
ART UNIT	PAPER NUMBER
2182	
MAIL DATE	DELIVERY MODE
07/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,266	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	Dean Phan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/21/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendments alter the scope of the claims. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of prior arts.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Schmidt (U.S Pub# 2002/0128037).

As to claim 16, Schmidt teaches a method comprising:

processing a first instruction of a first processor family instruction set in a host processor of a system (F. 2 CPU 220, par 29, *RISC instruction*); and

switching the system to process (par. 17, par. 33-34; *A multiplexer, instruction decoders function as a processor type select circuit which pass instruction to different elements of the core*) a first instruction of a second processor family instruction set in a

second core portion of a reconfigurable processor core coupled to the host processor (Fig. 1-2 reconfigurable core 150, par. 15), the reconfigurable processor core having a first core portion including a first plurality of processors configured to process instructions belonging to the first processor family instruction set (par. 15; *MIPS are in RISC family instruction set*) and the second core portion including a second plurality of processors configured to process instructions belonging to the second processor family instruction set (F.1-2, par15; ASIC, DSP); and

switching the system to process a second instruction of the first processor family instruction set after processing the first instruction of the second processor family instruction set (par. 29; *Since the processor 220 controls the system including wireless comm. 100, the first processor family instruction set must be processed before it switches to the second processor family set*).

As to claim 18, all elements of Claim 16 are listed, with further comprising: performing a plurality of wireless protocols using the first processor family instruction set and the second processor family instruction set (par 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-15, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt (U.S 2002/0128037), in view of Lee (US Pat# 5,490101).

As to claim 1, Schmidt discloses a circuit (Fig. 2) capable of supporting a plurality of host processor families comprising:

a host processor (Fig. 2 CPU 220) belonging to a first host processor family (par 29, RISC processor);

a reconfigurable processor core (Fig. 1-2 wireless comm 100, reconfigurable processor core 150, par. 15) coupled to the host processor (Fig.2 via bus 226), the reconfigurable processor core having a first core portion plurality of processors configured to process instructions belonging to the first host processor family (par. 15; MIPS is a RISC microprocessor) and a second core portion having a second plurality of processors configured to process instructions belonging to a second host processor family (DSP, or ASIC); and

a processor type select circuit (par. 16, 17; a multiplexer, instruction decoders) to configure the integrated circuit to process instructions belonging to an instruction set of one of the first or second host processor families (par. 17; *A multiplexer, instruction decoders function as a processor type select circuit which pass instruction to different elements of the core*).

Schmidt does not teach the host processor which is integrated in the disclosed circuit. However, in the same field of art, Lee teaches the concept of integrating plurality of digital data processing functions in a single chip. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to integrate the host

processor into the circuit of Schmidt, in order to reduce cost, low power consumption of the system. (*see col 1 lns 21-27; Also* MPEP 2144.04 (II) *in re Larson*).

As to claim 4, all limitation are in claim 1 with further: comprising an analog portion integrated on a substrate the analog portion including:

a cellular radio core; a radio sniffer coupled to the cellular radio core; a short rage wireless transceiver core coupled to the cellular radio core; (Schmidt, page 6 claim 1)

As to claim 5, all limitations of claim 4 are listed with further: the reconfigurable processor core adapted to handle a plurality of wireless communication protocols (Schmidt, paragraph 6).

As to claim 6, all limitations of claim 4 are listed with further: a memory array core coupled to the reconfigurable processor core (Schmidt, F. 1 memory 170, p. 14).

As to claims 7-15, all limitations of claim 5 are listed with further3 limitations in page 6 of Schmidt (Schmidt, page 6 claims 2-10).

As to claim 19, all elements are in claim 16 with further limitation in claim 1. Therefore, the claim is also rejected as claim 1.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being obvious over Schmidt (U.S 2002/0128037), in view of Lee (US Pat# 5,490101).

As to claim 2, 3, all limitations are listed in claim 1 with the reconfigurable processor core 150 can include one or more processors such as MIPS, DSP, ASIC, and others but does not specifically teach ARM processors. However, ARM processors have the same architecture as MIPS processors. Also, similar to MIPS, DSP, ASIC appliance

and use, ARM processors are one is one of the most popular processor in the world, especially in portable devices and computer peripherals. Therefore, it would have been obvious for one of ordinary skill in the art at the time of inventions to integrate ARM processor families into the reconfigurable core in order to improve and extend the utility, and compatibility of the core.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses an integrated circuit, which comprises a multiplexer, and plurality of selectable processors such as ARM and MIPS.

Pub# WO03005225 Stravers Paul "Processor Cluster"

or US Pub# 2004221136 as equivalent

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean Phan whose telephone number is (571) 270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dp

KIM HUYNH
SUPERVISORY PATENT EXAMINER
7/10/07